Amplitude Modulator Utilizing a High-Q Class-E DC-DC Converter

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Abstract **— A high-level amplitude modulator is designed and tested utilizing a high-Q Class-E DC-DC converter operating at a nominal switching frequency of 30 MHz. The output power is a maximum of 16.1 W and the efficiency is as high as 77.9%. The switching frequency is varied to control the output amplitude of the modulator. It is shown theoretically that the maximum useful dynamic range is 12.0 dB. An equation is derived that predicts the amount of frequency variation necessary to vary the output amplitude by a specific amount, based on the loaded Q of the circuit design. A RHP zero in the control-to-output transfer function is shown to have a detrimental effect on the modulation frequency to switching frequency ratio. The modulator is used to generate a DC-offset triangle-wave at frequencies as high as 500 kHz.**

I. INTRODUCTION

In communication systems employing digital modulation schemes, linear power amplifiers (LPAs) are required to meet stringent spectral regrowth requirements in order to avoid adjacent channel interference. For base station applications, LPAs typically operate in Class A or Class AB mode, and employ feedforward techniques. It is common to operate at low power levels for a large percentage of time. Linearly-biased PA efficiency can be quite poor under these circumstances, impacting cost, size and thermal management.

Several alternative designs have been proposed to circumvent the inherent tradeoff between linearity and efficiency. Two of these approaches have received considerable attention in recent papers, the Kahn Envelope Elimination & Restoration (EER) technique [1] and the dynamic carrier envelope tracking technique [2]-[4]. Both of these schemes utilize a high-level amplitude modulator to vary the DC supply voltage to the final stage, as shown in Fig. 1. An amplitude modulator can be implemented by rapidly changing the output level of a DC-DC converter in an efficient manner.

This paper investigates the high-frequency Class-E DC-DC converter for potential use as a high-level amplitude modulator. The converter shown in Fig. 2 is a Class-E amplifier [5], [6] driving its time-reversed companion, the Class-E (half-wave) rectifier [7]. This results in efficient operation at very high switching frequencies so that the output level can be controlled (modulated) very rapidly.

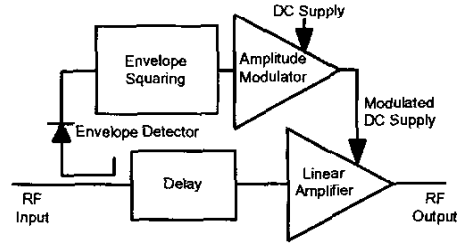

Fig. 1. Dynamic envelope tracking block diagram.

It is shown theoretically that a Class-E DC-DC converter (modulator) has a maximum useful dynamic range of 12.0 dB using variable frequency tuning. The theoretical efficiency is 83.5% or higher for a dynamic range of 10 dB. Based on the loaded Q of the design, an equation is derived that predicts the frequency shift needed to vary the output level by a specified amount [8]. The equation's accuracy is verified by the measured data.

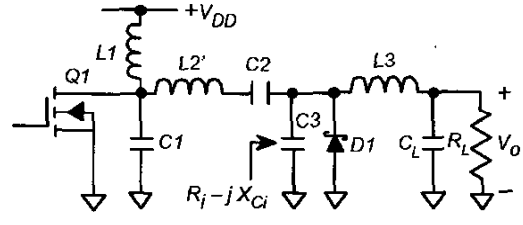

Fig. 2. Class-E DC-DC converter schematic. The polarity of diode $D1$ can be reversed to obtain a negative output voltage.

A modulator (Fig. 2) is designed and tested with a loaded Q of 12.5 at a nominal switching frequency of 30 MHz. The output power level is as high as 16.1 W at an efficiency of 77.9%. The switching frequency is varied to control the DC output level. For test purposes, the modulator is used to generate a DC-offset triangle-wave at the output, V_O, at frequencies as high as 500 kHz. The measured efficiency is 73%.

II. CONVERTER DESIGN

To allow for optimum performance at high switching frequencies, the Class-E amplifier is operated at a 50%

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duty-cycle with shunt capacitor *C1* set to its optimum value for a given value of load resistance [6]. The amplifier portion of the converter is "modulated" while the rectifier portion merely rectifies the sinusoidal output from the amplifier in an efficient manner.

Two methods are available to the designer for tuning the output network in order to modulate the output level. The output network component values (*L2* or *C2*) can be varied electronically [9] or the switching frequency can be varied [8], [10]. This paper explores the latter technique.

A. Design Analysis

The usual assumptions apply for the idealized analysis of the Class-E amplifier [5]. RF choke *L1* is large so that a constant DC current flows through it at all times. Active device *Q1* behaves as an ideal switch capable of current flow in either direction. The loaded Q (Q_L) is high enough to suppress harmonic currents in the output network.

In Fig. 3, power and efficiency are plotted versus output network tuning for the ideal case where the unloaded Q (Q_U) is infinite. Optimum operation occurs when X/R = 1.1525 at point "A". For the simple output network shown, a Class-E amplifier has a useful theoretical dynamic range of 12.0 dB, bounded by $0.2933 < X/R < 4.2941$. To the left of point "B" (peak power) the output power decreases. To the right of point "I" the input power begins to increase, so that tuning beyond this point is counterproductive. The efficiency is ~100% between points "A" and "D". Point "G" denotes the tuning location where the output power is 10 dB below that of point "B". Fig. 3 is applicable for *any* loaded Q, providing the high-Q assumption ($Q_L > \approx 5$) is satisfied for harmonic suppression.

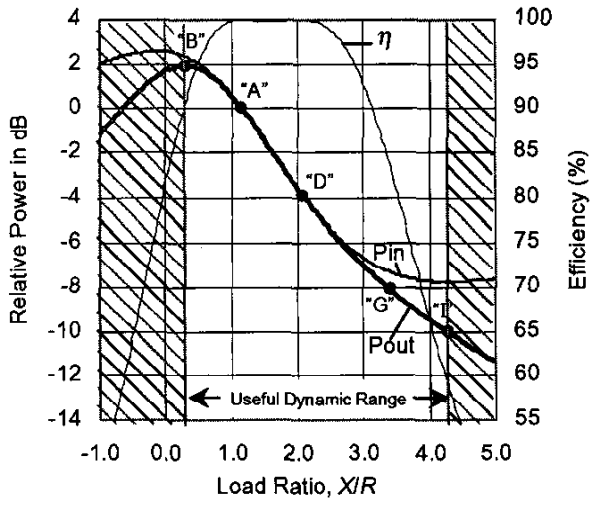

Fig. 3. Class-E amplifier power and efficiency versus load ratio tuning.

B. Circuit Implementation

The circuit of Fig. 2 was built using a Motorola MRF183S n-channel enhancement-mode RF power LDMOS FET. Measurements indicate that the dynamic on-resistance of the MRF183S is 0.194 Ω using a sinusoidal drive signal at 30 MHz. An experimental GaAs Schottky diode in a low-inductance package was used for *D1*. The circuit worked the first time as designed, and the classical waveforms for optimum operation were obtained. The loaded Q, the DC load resistance and the switching frequency were chosen to be $Q_L = 12.5$, $R_L = 14.0\,\Omega$ and $\omega_0/2\pi$ = 30 MHz, respectively. The unloaded Q of *L2* was measured to be 300 at 30 MHz. The component values were found to be $R_{load} \triangleq R_l = 8.075\,\Omega$, ($C3$ + C_{D1}) = 120.6 pF, C_l = 570.0 pF, ($C1$ + C_{DS}) = 115.6 pF, $C2$ = 55.5 pF, $L2$ = 558.8 nH, $L2'$ = 608.2 nH, $L1$ = 1.83 µH, $L3$ = 3.54 µH and C_L = 790 pF. ($L2'$ is substituted for $L2$ in Fig. 2 in order to compensate for C_l.) The theoretical best-case efficiency is 95% using the formula ($1 - Q_L/Q_U$). Greater detail regarding the design equations can be found in [8, ch. 10].

III. Variable Frequency Tuning Analysis

Variable frequency tuning has been investigated in the literature at 1 MHz for use in Class-E power supply design work [10], [11], but no theoretical equation exists to predict the amount of frequency shift needed. Until now it has been determined by experimental measurement. A theoretical equation is derived and verified in this section for the case where R_L is fixed. From a strictly technical standpoint, the design equations for optimum operation are not satisfied for variable frequency tuning because the value of *C1* is *fixed*—it is not changed as the frequency changes. Nevertheless, the circuit design is rather insensitive to the value of *C1* [6] and the analysis can be applied with excellent results.

A slight change in operating frequency can cause a significant change in output power. The goal is to determine a new "equivalent value" for the load ratio, X/R, due to a frequency shift from ω_0 to ω_0'. The load ratio is equal to the design value of 1.1525 for optimum operation when no frequency shift has occurred. This is the baseline reference. When the operating frequency is shifted to ω_0', the new value for X/R becomes

$$\left(\frac{X}{R}\right)' = \frac{X'_{L2} - X'_{C2}}{R} = \frac{\omega_0' L2 - (\omega_0' C2)^{-1}}{R}. \quad (1)$$

Using the design equations [8], this simplifies to

$$\left(\frac{X}{R}\right)' = \left(\frac{\omega_o'}{\omega_o} - \frac{\omega_o}{\omega_o'}\right) Q_L + \frac{\pi}{4}\left(\frac{\pi^2}{4} - 1\right)\frac{\omega_o}{\omega_o'}. \quad (2)$$

As Q_L increases, the sensitivity to a change in the operating frequency increases significantly. It is possible to solve for the normalized frequency, (ω_o'/ω_o), as a function of $(X/R)'$ and Q_L. A quadratic equation is solved involving (ω_o'/ω_o). This results in

$$\left(\frac{\omega_o'}{\omega_o}\right) = \frac{\left(\frac{X}{R}\right)'}{2Q_L} + \sqrt{\frac{1}{4Q_L^2}\left[\left(\frac{X}{R}\right)'\right]^2 - \frac{\pi}{4}\left(\frac{\pi^2}{4} - 1\right)\frac{1}{Q_L}} + 1. \quad (3)$$

To use this equation, a specific output power is selected and the corresponding value of X/R is determined from Fig. 3 or from the equations [8]. The tuning ratio has a useful range of $0.2933 < X/R < 4.2941$. This new value for the tuning ratio is given a prime designation, $(X/R)'$, to indicate that it is obtained by a frequency shift away from the nominal operating frequency. Once $(X/R)'$ is chosen, the value of the normalized frequency shift can be found for a particular value of loaded Q. A plot of (3) is shown in Fig. 4 for the case of tuning to points "B", "D", "G" and "I". It provides a convenient method to determine the required frequency shift versus Q_L to generate a different output power level.

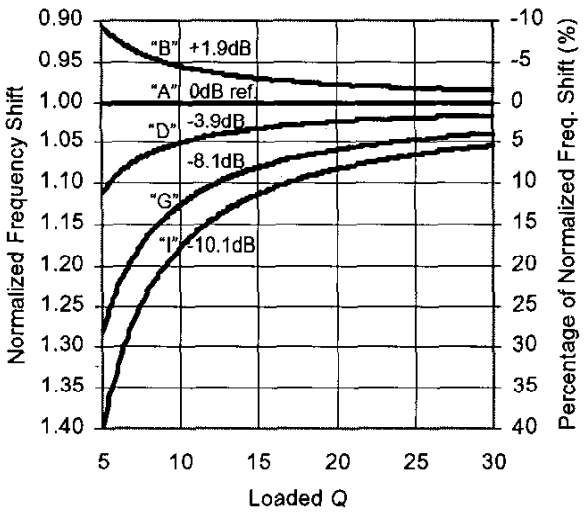

Fig. 4. Frequency shift tuning versus loaded Q.

For $Q_L = 12.5$, the predicted frequency shift is –3.541% to tune to point "B". This agrees closely with the experimentally measured frequency shift of –3.535%. The predicted frequency shift is +9.853% for tuning to point "G", versus an experimentally measured shift of +9.865%. The errors in the predictions are quite low at 0.006 and 0.012, respectively, and the accuracy improves as the loaded Q increases.

IV. Experimental Results

A. Static Performance

The measured efficiency of the amplifier portion is 90% for optimum operation, while the efficiency of the entire DC-DC converter is 77.9% at a maximum DC output power of 16.1 W. The power handling capability is limited by the 65 V drain-source breakdown voltage of the MRF183S.

The circuit was initially tested at a fixed DC supply voltage of V_{DD} = 10 Vdc. Power and efficiency data are plotted versus switching frequency in Fig. 5. Optimum performance occurs at 29.8 MIIz versus a target of 30.0 MHz, a design error of only 0.67%. The frequency is normalized to 29.8 MHz in Fig. 5. The efficiency is as high as 75.9% for V_{DD} = 10 Vdc. The voltage drop across $D1$ causes a noticeable "tilt" to the efficiency curve as shown. The diode loss can be quantified by [10]

$$P_{cond\ loss\ D1} = \frac{P_O}{P_O + P_D} = \frac{1}{1 + V_F/V_O}, \quad (4)$$

where V_F is the forward voltage across $D1$.

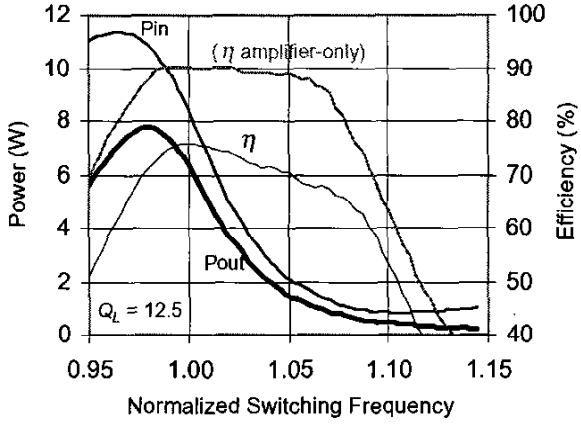

Fig. 5. Experimentally measured power and efficiency versus switching frequency.

B. Dynamic Performance

To demonstrate variable frequency tuning, the circuit was modulated over a dynamic range of approximately

10 dB by linearly sweeping the switching frequency up and down between 29.1 MHz and 32.2 MHz. This creates a test waveform consisting of a DC-offset triangle-wave at the output of the modulator. The gate of *Q1* was driven with an Agilent E4433B ESG-D RF signal generator with arbitrary waveform generation capability. (A VCO & PLL could be substituted.) Five "FM-triangular" test signals were created with five different repetition rates: 20, 50, 100, 200 and 500 kHz. The resulting modulator output voltages are shown in Fig. 6 and summarized in Table I.

Transient response data confirms the presence of a RHP zero, proportional to $(R_L/L1)$, in the control-to-output transfer function [12]. This prolongs the response time and limits performance at the higher modulating frequencies.

The control-to-output transfer function is not a linear function, so the triangle-wave produced by the modulator has a somewhat curved appearance. The DC output voltage is proportional to the square root of the amplifier's AC output power [8, ch. 11] and can be expressed as

$$V_O \propto \sqrt{P_{out}} = \sqrt{\frac{g^2 R V_{DD}^{\ 2}}{2 R_{dc}^{\ 2}}}. \qquad (5)$$

As a next step, the circuit could be linearized using pre-distortion and/or negative feedback.

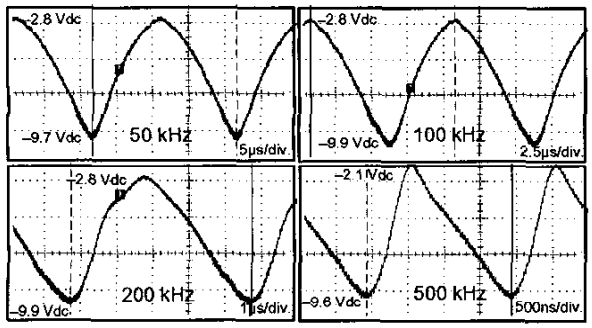

Fig. 6. Triangle-wave output from modulator at various modulation frequencies (repetition rates). In this example, *D1* is reversed so that the DC output voltage is negative. Vert: 2V/div.

TABLE I
MODULATOR PERFORMANCE VERSUS FREQUENCY

Triangle Frequency	Switching Frequency	Frequency Ratio	Efficiency	Dynamic Range	Comments
20 kHz	30 MHz	1 : 1500	72.6%	10.7 dB	Good
50 kHz	30 MHz	1 : 600	73.4%	10.7 dB	Good
100 kHz	30 MHz	1 : 300	73.9%	10.9 dB	Good
200 kHz	30 MHz	1 : 150	73.5%	10.9 dB	Distorted
500 kHz	30 MHz	1 : 60	73.0%	13.1 dB	Heavily Distorted

V. CONCLUSION

An amplitude modulator has been demonstrated using a high-Q Class-E DC-DC converter. It was shown that the maximum useful dynamic range is 12 dB for variable frequency tuning. A new expression (3) was derived that predicts the necessary frequency shift to vary the output level by a specified amount, based on the loaded Q of the design. A triangle-wave was generated with low distortion at frequencies up to 1/300th of the switching frequency, with an efficiency of 73.9%. By comparison, the best-case efficiency for amplifying a DC-offset triangle-waveform with a Class-A or a Class-B amplifier is 33.3% and 52.4%, respectively.

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